

# **LAYOUT DESIGN AND PROCESS TO FORM NANOTUBE CELL FOR NANOTUBE MEMORY APPLICATIONS**

## **ABSTRACT OF THE DISCLOSURE**

5           Nanotube memory cells are formed on a semiconductor substrate. Lower and  
upper memory cell chambers are formed by forming a first trench overlying the first  
and second contacts in a nitride layer, forming a second trench overlying the first and  
second contacts in a dielectric layer, depositing a nitride layer on the combined lower  
and upper chambers, and patterning the nitride layer to form an access hole to the  
10   nanotube layer and a second access hole to the second contact. A conductive layer is  
then deposited and patterned to form a top electrode contact and a nanotube layer  
contact. The conductive material closes the aperture created by the access hole.